**Refer to PL part inputs**.

FPGA SPECIFICATIONS

**Lior Yosef**

Date 22-01-2024

2024

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# ON COMMAND

YES

NO

YES

FB\_PG1   
FB\_PG2

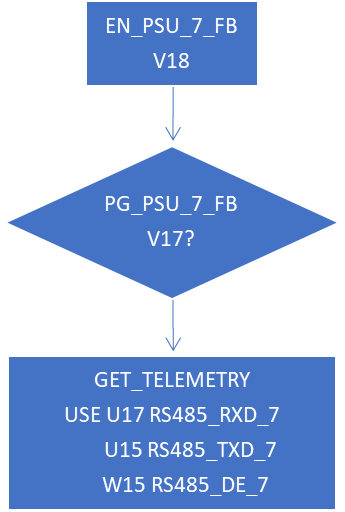
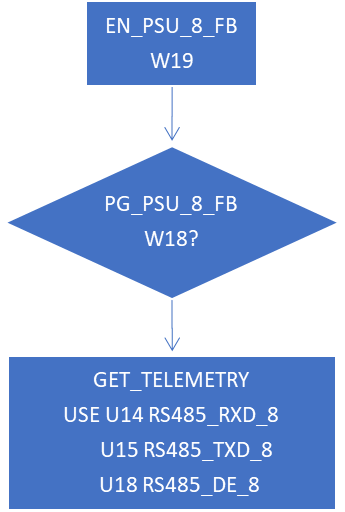
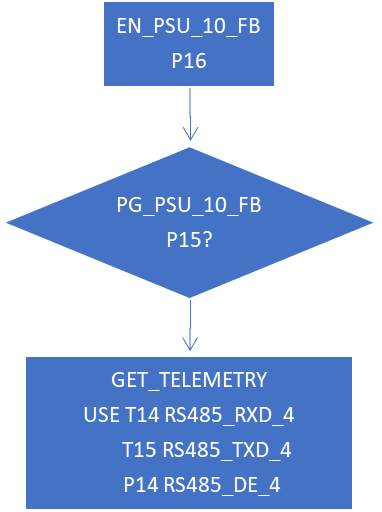
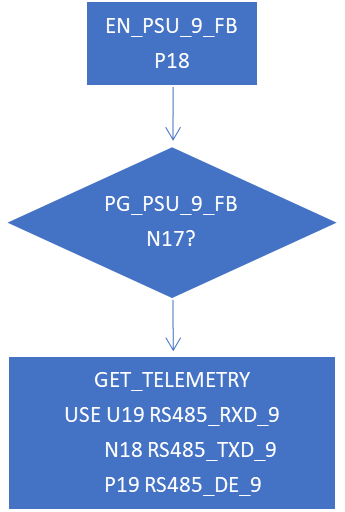
FB\_PG3

F

[CONTINUE TO ENABLE POWER SUPPLIES](#_ENABLE_POWER_SUPPLIES)

CONTINUE TO ENABLE FAN

# ENABLE POWER SUPPLIES



BUCK

USE V13 RS485\_RXD\_3

V12 RS485\_TXD\_3

W13 RS485\_DE\_3

**1msec after**

**All PG are ON:**

CCTCH\_INH\_FPGA G19

ECTCH\_INH\_FPGA H20

Go ON

# STATUS MESSAGAE

POD\_STATUS\_FPGA G17

Refer 3.1.6

LAMP\_STATUS\_FPGA J15

INPUT: if POD\_STATUS\_FPGA is HIGH

LAMP\_STATUS\_FPGA should be HIGH else 🡪 ERROR

# Voltage RMS Calculations

result 🡪 Vsns\_PH1, Vsns\_PH2, Vsns\_PH3

Sample frequency = 10kHz (AC FREQUENCY=400Hz, samples number=25, minimum samples number is 20)

CODE:

for (I=0; I<25; I++)

If (result>2048) {

sum+=new result

}

else {

sum+=new result

}

Rms input voltage =

**The result unit is VOLT.**

**1 - LSB = 0.109 Volt**

**==================================**

# Current RMS Calculations

# I\_sns

# Current Calculations

Offset🡪 every input has its offset calculated. see **Current offset measurement**

result 🡪 PH1\_I\_sns, PH2\_I\_sns, PH3\_I\_sns, DC\_PWR\_I\_sns

N 🡪 samples number

Sample frequency = 10kHz (AC FREQUENCY=400Hz, minimum samples number is 20)

CODE:

for (I=0;I<25;I++)

If (result>offset) {

sum+=new result

}

else {

sum+=new result

}

Rms input current =

**The result unit is Amper.**

**1 - LSB = 0.0147Amper**

# Current offset measurement

# 

Frequency 1kHz

## Current offset Calculations

Offset🡪 every input has its offset just as it read

result 🡪 PH1\_ZCR\_sns, PH2\_ZCR\_sns, PH3\_ZCR\_sns, DC\_PWR\_ZCR\_sns

no calculation is needed.

CODE:

result offset = result (the raw data)

## FAN Control

There are three Fans.

Each Fan has his own Outputs: enable, ctrl   
 and inputs: PG, Hall inputs.

The fan starts after getting ON\_COMMAND by driving high the enable.

Fan speed is controlled by FAN\_CTRLx\_FPGA

Fan speed is measured by FAN\_HALLx\_FPGA

Each fan sends the PG signal.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **FAN 1** | **FAN 2** | **FAN 3** |
| **FPGA Output** | FAN\_EN1\_FPGA | FAN\_EN2\_FPGA | FAN\_EN3\_FPGA |
| FAN\_CTRL1\_FPGA | FAN\_CTRL2\_FPGA | FAN\_CTRL3\_FPGA |
| **FPGA Inputs** | FAN\_PG1\_FPGA | FAN\_PG2\_FPGA | FAN\_PG3\_FPGA |
| FAN\_HALL1\_fpga | FAN\_HALL2\_fpga | FAN\_HALL3\_fpga |
| **FAN\_CTRL\_FPGA center frequency 50% duty cycle** | 1Khz | 0.9Khz | 0.8Khz |
| **Target Fan speed “RPM” measured by FAN\_HALL ± 2%** | 10471.2 | 13015.1 | 12145.7 |
| **Per second** | 174.5 ± 2% | 216.9 ± 2% | 202.4 ± 2% |

Increase/decrease the frequency to control fan speed (RPM) to be in the desired speed ±2%

Final working frequency will be declared at integration time.

Stabilization time assume as 3sec.

SHUTDOWN\_OUT\_FPGA G15

Refer to 3.1.5.2 for shutdown when system power of (named power down)

Refer to 3.2.10.2.1 to create shut down in over voltage for input voltage.

Refer to 3.2.10.5 to create shut down in over temperature.

ESHUTDOWN\_OUT\_FPGA K14

Refer to 3.2.10.2 for the case of outputs over voltage.

RESET\_OUT\_FPGA H15   
 refer to 3.1.5.1 System Reset (“short” reset)

## VCC\_12V\_REDUNDANT POWER DOWN ALARM

100Hz sampling

NO

YES

NO

YES

## POD STATUS FPGA(LOW) CHECK USING LAMP STATUS

NO

## [POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS](#_POD_STATUS_FPGA(HIGH)_1)

NO

YES

YES

## POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS

CHECK 3 TIMES